WHAT IS CLAIMED IS:

1. A semiconductor device with an OTP ROM formed over a semiconductor substrate including a memory cell area and a peripheral circuit area, the semiconductor device comprising:

a MOS transistor having a floating gate electrode, the MOS transistor being disposed at the memory cell area;

an OTP ROM capacitor having a lower electrode, an upper intermetal dielectric, and an upper electrode which are stacked in the order named, the OTP ROM capacitor being disposed over the MOS transistor; and

a floating gate plug connecting the floating gate electrode with the lower electrode,

wherein the floating gate electrode, the floating gate plug, and the lower electrode constitute a conductive structure which is electrically insulated.

2. The semiconductor device as set forth in claim 1, further comprising a capacitor that is disposed in the peripheral circuit area and includes a lower capacitor electrode, a dielectric film, and an upper capacitor electrode which are stacked in the order named.

3. The semiconductor device as set forth in claim 2, wherein the lower electrode and the upper electrode are identical to the lower capacitor electrode and the upper capacitor electrode in material and thickness.

4. The semiconductor device as set forth in claim 2, wherein the upper intermetal dielectric and the dielectric film are identical in material and thickness.

5. The semiconductor device as set forth in claim 1, wherein the upper intermetal dielectric is made of at least one selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.

6. The semiconductor device as set forth in claim 1, wherein the upper intermetal dielectric is disposed over an entire surface of the semiconductor substrate.

7. The semiconductor device as set forth in claim 2, further comprising a lower intermetal dielectric formed below the upper intermetal dielectric.

8. The semiconductor device as set forth in claim 7, wherein the lower intermetal dielectric forms an OTP ROM opening and the upper electrode is formed in the OTP ROM opening.

9. The semiconductor device as set forth in claim 2, wherein the lower intermetal dielectric forms a capacitor opening and the upper capacitor is formed in the capacitor opening.

10. The semiconductor device as set forth in claim 1, further comprising a contact plug which is connected to an impurity region of the semiconductor substrate and is made of the same material as the floating gate plug.

11. The semiconductor device as set forth in claim 10, further comprising a bitline, the contact plug connecting the bitline to the impurity region of the semiconductor substrate.

12. The semiconductor device as set forth in claim 1, wherein the upper electrode comprises a first upper electrode and a second upper electrode disposed over the first upper electrode.

13. The semiconductor device as set forth in claim 2, wherein the upper capacitor electrode comprises a first upper capacitor electrode and a second upper capacitor electrode disposed over the first upper capacitor electrode.

14. A method of fabricating a semiconductor device with an OTP ROM, comprising:

forming a floating gate electrode over a semiconductor substrate;

forming a lower electrode electrically connected to the floating gate electrode;

forming an upper intermetal dielectric over an entire surface of the semiconductor substrate including the lower electrode; and

forming an upper electrode over the upper intermetal dielectric.

15. The method as set forth in claim 14, before formation of the floating gate electrode, further comprising:

forming a device isolation layer at a predetermined region of the semiconductor substrate to define an active region; and

forming a gate insulating layer at the active region.

16. The method as set forth in claim 14, wherein the formation of the lower electrode comprises:

forming an interlayer dielectric over an entire surface of the semiconductor substrate including the floating gate electrode;

patterning the interlayer dielectric to form a floating gate contact hole exposing a top surface of the floating gate electrode;

forming a floating gate plug to fill the floating gate contact hole;

forming a lower conductive layer on an entire surface of the semiconductor substrate including the floating gate plug; and

patterning the lower conductive layer to form the lower electrode electrically connected to the floating gate plug.

17. The method as set forth in claim 14, wherein the floating gate electrode, the floating gate plug and the lower electrode form an electrically insulated conductive structure.

18. The method as set forth in claim 14, before formation of the upper intermetal dielectric, further comprising:

forming a lower intermetal dielectric over an entire surface of the semiconductor substrate including the lower electrode; and

patterning the lower intermetal dielectric to form an OTP ROM opening exposing a top surface of the lower electrode.

19. The method as set forth in claim 14, wherein the upper intermetal dielectric is made of at least one selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

20. The method as set forth in claim 14, wherein the upper intermetal dielectric is used as an etch-stop layer during a process for forming the upper electrode.

21. The method as set forth in claim 14, wherein the intermetal dielectric remains on an entire surface of the semiconductor substrate after the formation of the upper electrode.

22. A method of fabricating a semiconductor device with an OTP ROM disposed at a semiconductor substrate including a memory cell area and a peripheral circuit area, the method comprising:

forming a floating gate electrode over the memory cell area of the semiconductor substrate;

simultaneously forming a lower electrode electrically connected to the floating gate electrode over the memory cell area and a lower capacitor electrode disposed over the peripheral circuit area;

forming a dielectric film over an entire surface of the semiconductor substrate including the lower electrode and the lower capacitor electrode; and

simultaneously forming an upper electrode and an upper capacitor electrode over the dielectric film, the upper electrode crossing over the lower electrode and the upper capacitor electrode crossing over the lower capacitor electrode.

23. The method as set forth in claim 22, before formation of the floating gate electrode, further comprising:

forming a device isolation layer at a predetermined region of the semiconductor substrate to define an active region; and

forming a gate insulating layer at the active region.

24. The method as set forth in claim 22, before formation of the lower electrode and the lower capacitor electrode, further comprising:

forming an interlayer dielectric over an entire surface of the semiconductor substrate including the floating gate electrode;

patterning the interlayer dielectric to form a floating gate contact hole exposing a top surface of the floating gate electrode; and

forming a floating gate plug to fill the floating gate contact hole.

25. The method as set forth in claim 24, wherein the formation of the lower electrode and the lower capacitor electrode comprises:

forming a lower conductive layer over an entire surface of the semiconductor substrate including the floating gate plug; and

patterning the lower conductive layer to form the lower electrode electrically connected to the floating gate plug,

wherein the lower electrode, the floating gate plug, and the floating gate electrode constitute a conductive structure that is electrically insulated.

26. The method as set forth in claim 22, before formation of the dielectric film, further comprising:

forming a lower intermetal dielectric over an entire surface of the semiconductor substrate including the lower electrode and the lower capacitor electrode; and

patterning the lower intermetal dielectric to form an OTP ROM opening exposing a top surface of the lower electrode and a capacitor opening exposing a top surface of the lower capacitor electrode.

27. The method as set forth in claim 22, wherein the upper intermetal dielectric is made of at least one selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

28. The method as set forth in claim 22, wherein the upper intermetal dielectric is used as an etch-stop layer during a process for forming the upper electrode and the upper capacitor electrode.

29. The method as set forth in claim 22, wherein the upper intermetal dielectric remains on the entire surface of the semiconductor substrate after formation of the upper electrode and the upper capacitor electrode .